1. A method comprising:

forming a gate structure over a semiconductor substrate;

using a plasma to clean the gate structure; and

forming a portion of source drain junction using plasma doping at energies of less than approximately 100 eV.

2. The method of claim 1 wherein using plasma includes using hydrogen plasma to clean the gate structure.

3. The method of claim 1 wherein using plasma to clean includes using plasma at energies of less than approximately 100 eV.

4. The method of claim 1 including forming a source drain extension using plasma doping.

5. The method of claim 1 including covering the gate structure to reduce the loss of impurities from the gate structure.

6. A method comprising:

using plasma doping at energies of less than approximately 100 eV to dope a gate structure with impurities; and

covering the structure to reduce the loss of the impurities from the gate structure.

7. The method of claim 6 including using plasma to clean the gate structure prior to doping the gate structure.

8. The method of claim 6 wherein covering the structure includes covering the structure with doped glass.

9. The method of claim 6 including forming a source drain region using plasma doping.

10. The method of claim 9 wherein covering the structure includes covering both a gate and source drain regions.

11. The method of claim 6 including forming a PMOS transistor.

12. The method of claim 6 including plasma doping using boron.

13. The method of claim 6 including controlling the plasma doping to cause the gate structure top and sides to be doped to substantially the same extent.

14. The method of claim 6 including diffusing and activating the impurities using rapid thermal annealing.

15. A semiconductor structure comprising:

a substrate;

a plasma doped gate material formed on said substrate;

plasma doped source drain extensions formed adjacent said gate material; and

a cover over said plasma doped gate material and said source drain extensions to reduce the loss of plasma doped impurities.

16. The structure of claim 15 wherein gate material has a top and sides, said sides being closer to said source drain extensions, said top and sides being doped to substantially the same extent.

17. The structure of claim 15 wherein doped gate material includes polysilicon.

18. The structure of claim 15 wherein said cover is formed of doped glass.

19. The structure of claim 15 wherein said doping is a p-type doping.